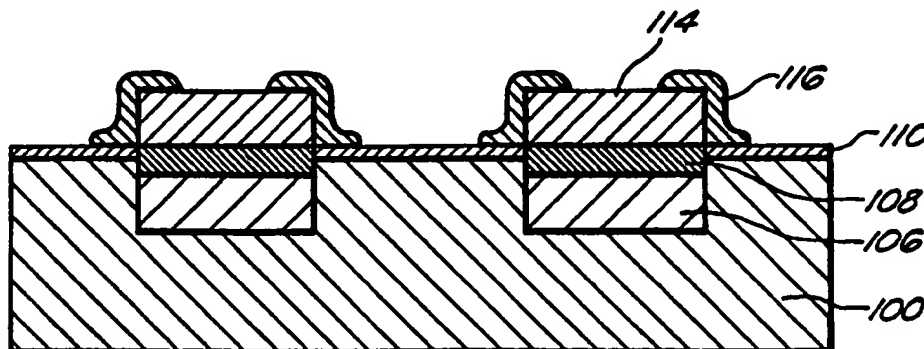




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : H01L 21/8258	A1	(11) International Publication Number: WO 99/14804 (43) International Publication Date: 25 March 1999 (25.03.99)
(21) International Application Number: PCT/US98/18715 (22) International Filing Date: 8 September 1998 (08.09.98) (30) Priority Data: 60/059,091 16 September 1997 (16.09.97) US (71) Applicant: MASSACHUSETTS INSTITUTE OF TECHNOLOGY [US/US]; 77 Massachusetts Avenue, Cambridge, MA 02139 (US). (72) Inventor: FITZGERALD, Eugene, A.; 7 Camelot Road, Windham, NH 02652 (US). (74) Agents: CONNORS, Matthew, E. et al.; Samuels, Gauthier, Stevens & Reppert, Suite 3300, 225 Franklin Street, Boston, MA 02110 (US).		(81) Designated States: CA, JP, KR, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published With international search report.

(54) Title: CO-PLANAR Si AND Ge COMPOSITE SUBSTRATE AND METHOD OF PRODUCING SAME



(57) Abstract

A semiconductor structure including a silicon wafer having silicon regions, and at least one $\text{Ge}_x\text{Si}_{1-x}$ region integrated within the silicon regions. The silicon and $\text{Ge}_x\text{Si}_{1-x}$ regions can be substantially co-planar surfaces. The structure can include at least one electronic device configured in the silicon regions, and at least one electronic device of III-V materials configured in said at least one $\text{Ge}_x\text{Si}_{1-x}$ region. The structure can be, for example, an integrated III-V/Si semiconductor microchip. In accordance with another embodiment of the invention there is provided a method of fabricating a semiconductor structure, including providing a silicon wafer with a surface; forming a pattern of vias within the surface of the wafer; and depositing regions of $\text{Ge}_x\text{Si}_{1-x}$ within the vias. The method can include the step of processing the wafer so that the wafer and $\text{Ge}_x\text{Si}_{1-x}$ regions have substantially co-planar surfaces. Another embodiment provides a method of fabricating a semiconductor structure, including providing a silicon wafer with a surface; depositing regions of $\text{Ge}_x\text{Si}_{1-x}$ to the surface of the silicon wafer; and depositing silicon to the surface such that the deposited $\text{Ge}_x\text{Si}_{1-x}$ regions are integrated within silicon.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav	TM	Turkmenistan
BF	Burkina Faso	GR	Greece		Republic of Macedonia	TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's	NZ	New Zealand		
CM	Cameroon		Republic of Korea	PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakhstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LI	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

CO-PLANAR Si and Ge COMPOSITE SUBSTRATE AND METHOD OF PRODUCING SAME

BACKGROUND OF THE INVENTION

5 The invention relates to the field of lattice-mismatched semiconductor material integration, and in particular to the integration of SiGe materials onto a Si substrate.

As many lattice-matched devices and circuits mature, interest in lattice-mismatched semiconductors, devices, and circuits has increased. There are two driving forces behind the increased commercial interest: integration and component performance. Integrating
10 dissimilar semiconductor materials on a common substrate allows the designer to improve performance, lower cost, and increase reliability. Thus, the most susceptible applications to this initial advance will be systems that require multiple types of semiconductor materials currently packaged separately and combined in a more conventional packaging solution. Examples of these applications are III-V materials integration on Si, and SiGe circuit
15 integration with Si CMOS. Such single-chip systems are anticipated to have wide application in communication technologies, particularly wireless communications technologies.

The utility of combined dissimilar semiconductors relies on the quality of the resulting material. Large lattice-mismatch between the substrate and deposited layer creates
20 stress during material deposition, creating many defects in the deposited layer, resulting in poor material quality and limited performance. To control threading dislocation densities in high mismatched deposited layers, there are only two well-established techniques: substrate patterning and composition grading. In the case of substrate patterning, the idea utilizes the knowledge that the threading dislocations are a necessity of geometry, i.e. that
25 a dislocation cannot end in a crystal. If the free edge is brought closer to another free edge by patterning the substrate into smaller growth areas, then it is possible to reduce threading dislocation densities. This technique works best for low mismatched systems in which dislocation nucleation is not rampant; however, it will reduce threading dislocation densities in high mismatched systems as well.

30 The other well-established technique is the use of composition graded layers. One can imagine that to reach a large total mismatch, a series of low mismatched interfaces

-2 -

could achieve great relaxation but keep threading dislocation densities low. This result is possible if each layer becomes substantially relaxed and is able to reuse the threading dislocations from the layer below. This method was long ago applied in an empirical way to GaAsP LEDs grown on lattice-mismatched GaAs substrates. However, after the GaAsP
5 process was transferred to manufacturing, most of the subsequent lattice-mismatch research focussed on single mismatched interfaces. The driving force for lattice-mismatched materials in applications decreased as AlGaAs/GaAs structures and InGaAsP/InP structures dominated optoelectronic and electronic device applications. Until these materials systems were fully exploited, the implementation of high mismatched layers seemed unnecessary.

10 A renewed interest in graded layers has occurred due to the increased demand for novel components, as well as an increased demand for increased integration. The advances in relaxed graded SiGe have shown that SiGe devices based on relaxed SiGe on Si, and the integration of III-V materials on Si using intermediate relaxed SiGe graded layers are possible. Thus, relaxed, graded SiGe layers can act as the material bridge between SiGe
15 devices and/or III-V devices and Si substrates.

These materials advances, however, are incomplete unless a proper process sequence can be found to create these relaxed layers and subsequent devices with relatively standard Si circuit processing. A critical view of electronic and optoelectronic systems shows that the main data processing in many applications can be executed in Si CMOS
20 circuits, which dominate the semiconductor industry today. To create a new realm of Si-based single-chip systems, a structure and process to combine Si CMOS circuits with the materials advances in relaxed graded SiGe mentioned above, is necessary.

25

SUMMARY OF THE INVENTION

The invention provides a method of producing a co-planar SiGe/Si substrate. The SiGe regions are formed using relaxed graded SiGe technology. The planarization process described below creates a modified Si wafer which can proceed through the Si CMOS process. At a convenient point in the CMOS process, the devices on or in the SiGe regions
30 can be metallized and connected to the CMOS circuit, creating a single-chip system utilizing Si devices, SiGe devices, and/or III-V devices.

The invention also provides a semiconductor structure and method for producing such a structure in which relaxed GeSi crystalline alloy surfaces can co-exist in a planar fashion with Si. Such a substrate is essential in harnessing the plethora of applications in which the integration of GeSi materials and devices, and/or III-V materials and devices
5 grown on GeSi, with Si electronics is desired.

Accordingly, in accordance with one embodiment of the invention there is provided a semiconductor structure comprising a silicon wafer having silicon regions, and at least one $\text{Ge}_x\text{Si}_{1-x}$ region integrated within the silicon regions. The silicon and $\text{Ge}_x\text{Si}_{1-x}$ regions can be substantially coplanar surfaces. The structure can include at least one electronic device
10 configured in the silicon regions, and at least one electronic device of III-V materials configured in the at least one $\text{Ge}_x\text{Si}_{1-x}$ region. The structure can be, for example, an integrated III-V/Si semiconductor microchip.

In accordance with another embodiment of the invention there is provided a method of fabricating a semiconductor structure, comprising providing a silicon wafer with a
15 surface; forming a pattern of vias within the surface of the wafer; and depositing regions of $\text{Ge}_x\text{Si}_{1-x}$ within the vias. The method can include the step of processing the wafer so that the wafer and $\text{Ge}_x\text{Si}_{1-x}$ regions have substantially coplanar surfaces. Another embodiment provides a method of fabricating a semiconductor structure, comprising providing a silicon wafer with a surface; depositing regions of $\text{Ge}_x\text{Si}_{1-x}$ to the surface of the silicon wafer; and
20 depositing silicon to the surface such that the deposited $\text{Ge}_x\text{Si}_{1-x}$ regions are integrated within silicon.

These and other objects, features and advantages of the present invention will become apparent in light of the following detailed description of preferred embodiments thereof, as illustrated in the accompanying drawings.

25

BRIEF DESCRIPTION OF THE DRAWINGS

FIGs. 1A-1E are a series of side views of a semiconductor structure illustrating the process of producing a wafer of a substrate that possesses both GeSi alloys and Si at
30 the surface in accordance with the invention; and

FIG. 2 is a top view of an exemplary co-planar Si electronics/GeSi composite

substrate configured as a microchip.

DETAILED DESCRIPTION OF THE INVENTION

5 FIGs. 1A-1E are a series of side views of a semiconductor structure illustrating the process of producing a wafer of a substrate that possesses both GeSi alloys and Si at the surface in accordance with the invention. FIG. 1A illustrates the first process step which involves initially patterning a conventional Si wafer 100. Such a wafer is usually a (001) orientated wafer, in which the off-cut of an (001) wafer is induced by polishing the wafer
10 6 degrees towards the [110] direction. The Si wafer should be patterned lithographically and masked such that vias 102 can be etched into the wafer. These vias will be the areas where the GeSi material will be deposited.

For example, the Si wafer can be coated with a layer 104 of SiO₂, covered with photoresist, and lithographically developed, producing the desired pattern in the wafer. HF-
15 water or buffered etched solutions can be used then to remove the oxide from the areas in which the photoresist was removed. Finally, after the photoresist is removed, the Si vias 102 can be formed by immersing the wafer in an etch solution, such as KOH, which does not etch SiO₂. The result is the formation of the Si vias. If more vertical side-walls are desired, for example, a dry etch can be used instead of the KOH etch step.

20 The wafer can then be cleaned to insure that no contamination is carried from the etch step into the rest of the process. The wafer is then inserted into a GeSi deposition system, such as a chemical vapor deposition system. As shown in FIG. 1B, a graded GeSi layer 106 is deposited such that the Ge composition is graded over the thickness of the material in the vias 102. At the end of the graded region, a uniform composition GeSi layer
25 108 of the desired composition is grown such that the growth surface traverses the Si surface before the end of growth. This requirement will ensure that the GeSi growth in the via extends above the surface of the Si wafer, and also ensures that the subsequent planarization step does not extend into the composition graded region, located below the uniform layer.

30 The conditions used for the growth of SiGe should be consistent with optimal growth conditions for relaxed, SiGe graded structures. For example, graded layers grown

- 5 -

to alloy concentrations of 30% Ge are typically grown in UHVCVD at temperatures approximately 750-800C, and under reactor pressures of 25mT. Grading rates are typically 10% Ge per μm or less.

As shown in FIG. 1C, the wafer can then be chemo-mechanically polished back, so that the uniform GeSi regions 108 are co-planar with the Si surface. If the oxide layer is not removed for the polishing step, it can be used as a control in the polishing process. The change in colors as the wafer is polished will signal the approach of the Si wafer surface. When the Si surface is reached, the polishing can be ceased since the surface is co-planar.

It will be appreciated that with this substrate, it is now possible to insert the wafer into a conventional Si electronics (CMOS) production line and process the Si areas for Si electronics. The only restriction is that the Si CMOS process might be modified to reduce the temperatures of the highest temperature steps. This process may be required for the high-Ge alloys, such as 70-100% Ge in GeSi alloys. The melting point of these alloys approaches that of Ge, which is 936 C. Thus, if the GeSi alloy layer is graded to 100% Ge, the Si CMOS processing temperatures should be reduced so that the Ge layer is not damaged significantly.

It will also be appreciated that other advances in improved graded SiGe structures using planarization and/or CMP can be combined with this invention to improve the SiGe material quality. For example, the process described here can be used to create co-planar 50% Ge alloys with Si. Subsequent continued graded layer growth on the SiGe areas will result in improved SiGe alloys with high Ge concentrations on top of the SiGe via regions.

Examples of applications are the integration of GeSi transistors with traditional Si CMOS circuits and devices. In this case, the GeSi areas may be graded to 30% Ge, and the processing temperatures of the Si CMOS process would only have to be marginally modified.

As shown in FIG. 1E, the Si CMOS electronics are shown as regions 110, and can include, for example, SI transistors and conventional interconnects therebetween. In the case of integrated III-V devices with Si CMOS, the alloys are generally graded to much higher lattice constants, e.g. 70-100% Ge. These higher Ge concentrations have larger lattice constants, and are therefore lattice-matched to some of the III-V materials. Also, in this case, it is imperative to use off-cut wafers at the initiation of the process, as described

above.

During CMOS fabrication on the Si areas, the GeSi areas can be covered with SiO₂ during the entire process. After the Si CMOS is fabricated, the areas above the GeSi can be exposed and the Si CMOS or electronics can be protected with a passivating mask layer
5 112 of oxide or nitride. Once the GeSi areas are exposed, layers 114 of III-V materials can be deposited, as shown in FIG. 1E. One must be careful in initiating the GaAs growth on Ge correctly in order to prevent high dislocation densities from forming in the GaAs layer.

After III-V growth, the material can be defined or etched (the mask is dissolved and lifted-off), and final metallization can occur in which the III-V devices are connected to each
10 other and also the Si electronics via interconnects 116, thus forming an integrated III-V/Si chip.

FIG. 2 is a top view of an exemplary co-planar Si electronics/GeSi composite substrate configured as a microchip 120. The chip includes a GeSi region 122 fabricated as described heretofore, and a Si CMOS circuit region 124 connected to the GeSi region
15 by interconnects 126.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

20 What is claimed is:

CLAIMS

- 1 1. A semiconductor structure comprising:
2 a silicon wafer having silicon regions; and
3 at least one $\text{Ge}_x\text{Si}_{1-x}$ region integrated within said silicon regions.
- 1 2. The semiconductor structure of claim 1, wherein said silicon and $\text{Ge}_x\text{Si}_{1-x}$ regions
2 comprise substantially coplanar surfaces.
- 1 3. The semiconductor structure of claim 1 further comprising at least one electronic
2 device configured in said silicon regions.
- 1 4. The semiconductor structure of claim 1 further comprising at least one electronic
2 device of III-V materials configured in said at least one $\text{Ge}_x\text{Si}_{1-x}$ region.
- 1 5. The semiconductor structure of claim 1 further comprising at least one electronic
2 device of III-V materials configured in said at least one $\text{Ge}_x\text{Si}_{1-x}$ region.
- 1 6. An integrated III-V/Si semiconductor microchip, comprising:
2 a silicon wafer having silicon regions;
3 at least one electronic device configured in said silicon regions;
4 at least one $\text{Ge}_x\text{Si}_{1-x}$ region integrated within said silicon regions; and
5 at least one electronic device of III-V materials configured in said at least one
6 $\text{Ge}_x\text{Si}_{1-x}$ region.
- 1 7. An integrated GeSi/Si semiconductor microchip, comprising:
2 a silicon wafer having silicon regions;
3 at least one electronic device configured in said silicon regions;
4 at least one $\text{Ge}_x\text{Si}_{1-x}$ region integrated within said silicon regions; and
5 at least one electronic device of GeSi material configured in said at least one
6 $\text{Ge}_x\text{Si}_{1-x}$ region.

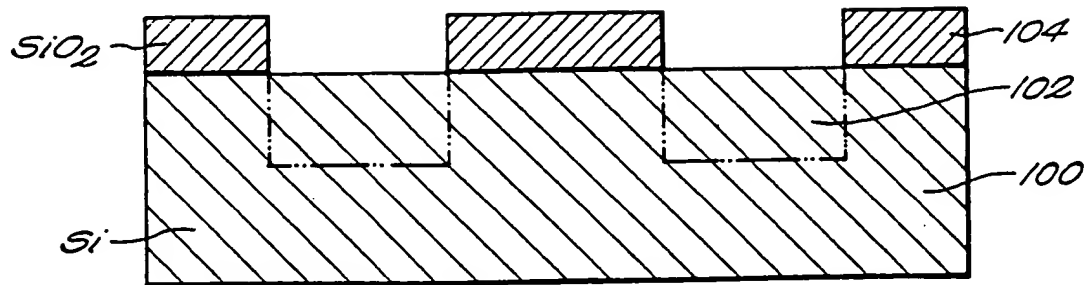
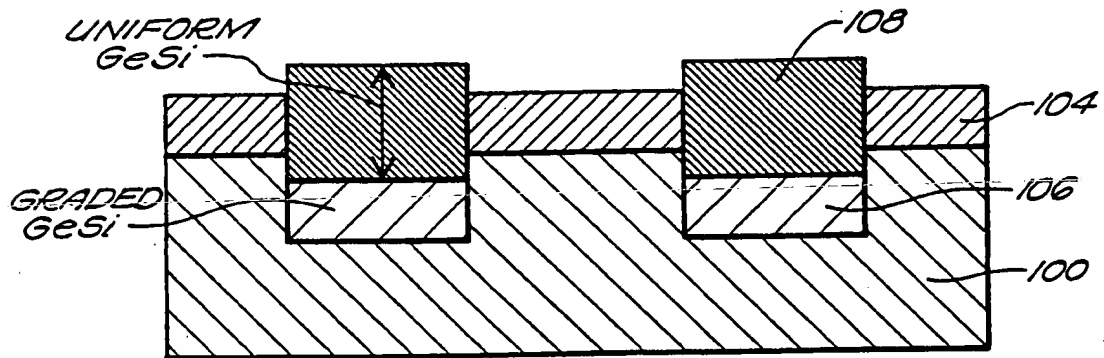
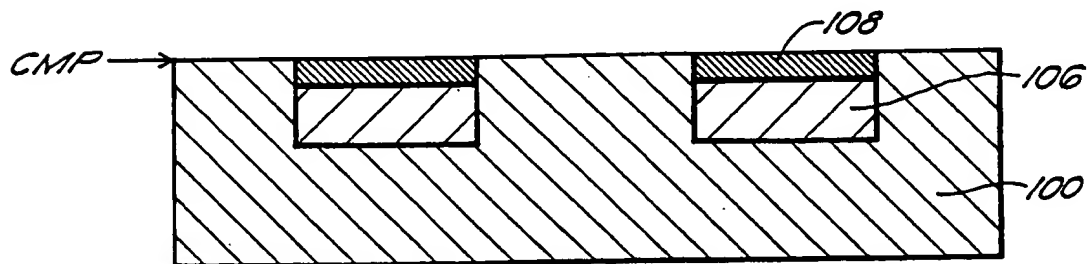
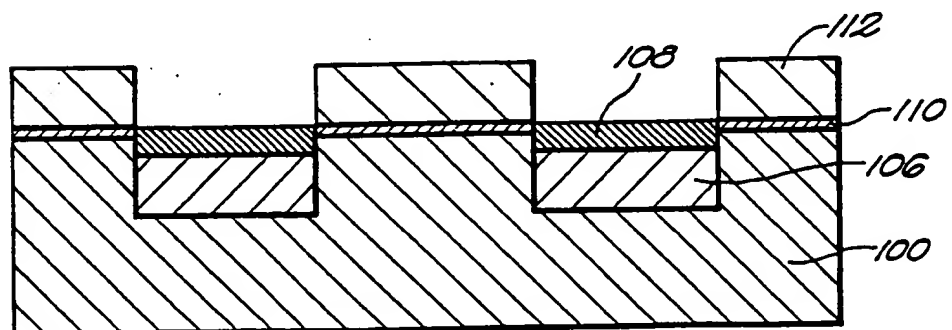
-8 -

1 8. A method of fabricating a semiconductor structure, comprising:
2 providing a silicon wafer with a surface;
3 forming a pattern of vias within the surface of said wafer; and
4 depositing regions of $\text{Ge}_x\text{Si}_{1-x}$ within said vias.

1 9. The method of claim 8 further comprising processing said wafer so that said
2 wafer and $\text{Ge}_x\text{Si}_{1-x}$ regions have substantially coplanar surfaces.

1 10. A method of fabricating a semiconductor structure, comprising:
2 providing a silicon wafer with a surface;
3 depositing regions of $\text{Ge}_x\text{Si}_{1-x}$ to said surface of said silicon wafer; and
4 depositing silicon to said surface such that said deposited $\text{Ge}_x\text{Si}_{1-x}$ regions are
5 integrated within silicon.

1 / 2

**FIG. 1A****FIG. 1B****FIG. 1C****FIG. 1D**

2 / 2

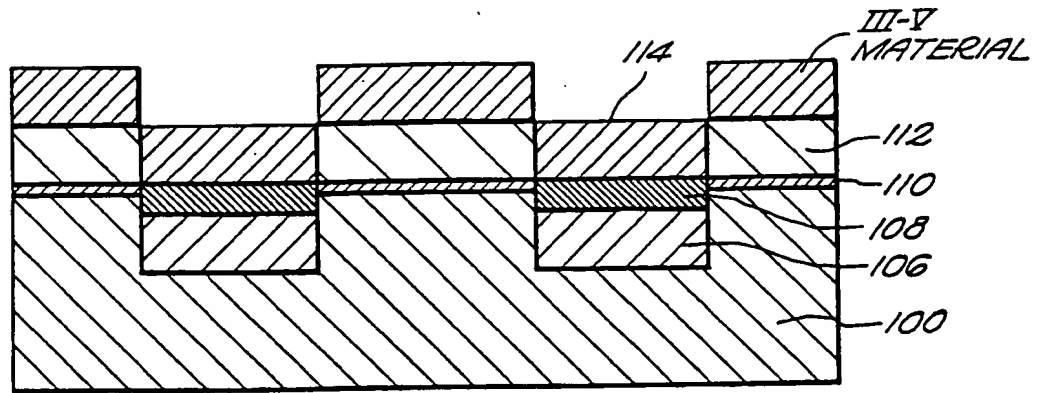


FIG. 1E

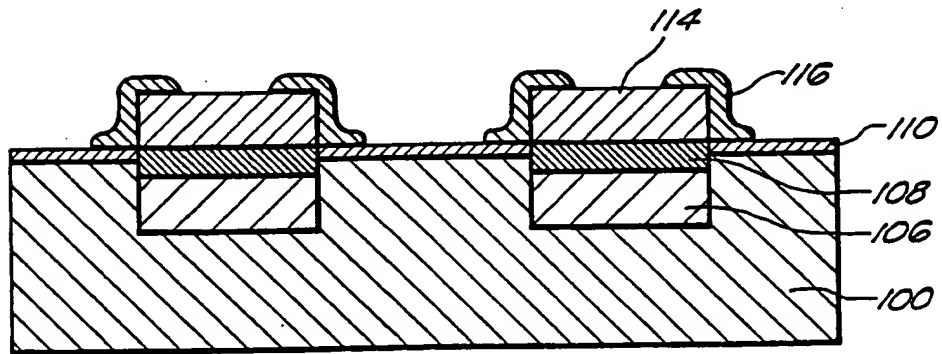


FIG. 1F

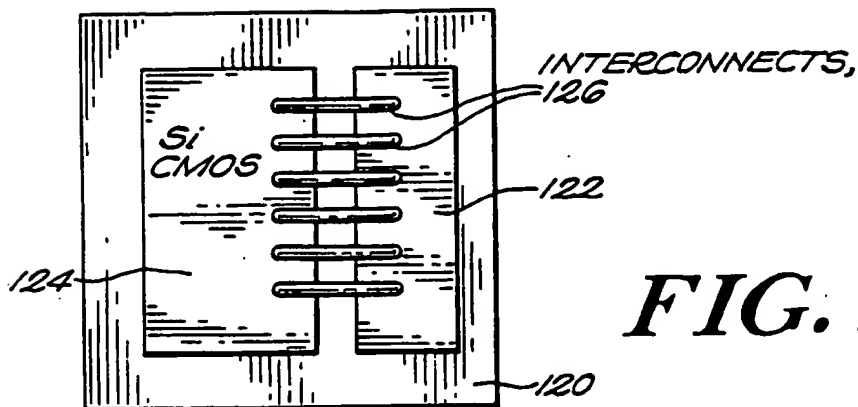


FIG. 2

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 98/18715

A. CLASSIFICATION OF SUBJECT MATTER
 IPC 6 H01L21/8258

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 514 018 A (AMERICAN TELEPHONE & TELEGRAPH) 19 November 1992 see the whole document	1-10
X	CHANG Y: "FABRICATION OF PATTERNED GEXSII-X/SI LAYERS BY PULSED LASER INDUCED EPITAXY" APPLIED PHYSICS LETTERS, vol. 58, no. 19, 13 May 1991, pages 2150-2152, XP000216321 cited in the application	1,2,10
A	see the whole document -- -/--	3,7-9

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"S" document member of the same patent family

Date of the actual completion of the international search

26 November 1998

Date of mailing of the international search report

03/12/1998

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
 NL - 2280 HV Rijswijk
 Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
 Fax: (+31-70) 340-3016

Authorized officer

Albrecht, C

INTERNATIONAL SEARCH REPORT

Inte. J. onal Application No

PCT/US 98/18715

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	"MONOLITHIC PROCESS FOR CO-INTEGRATION OF GAAS AND SILICON CIRCUITS" INTERNATIONAL ELECTRON DEVICES MEETING, SAN FRANCISCO, DEC. 11 - 14, 1988, 11 December 1988, pages 778-781, XP000013461 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS see the whole document -----	1-10
A	US 3 905 037 A (BEAN KENNETH E ET AL) 9 September 1975 see the whole document -----	1-10

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 98/18715

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0514018 A	19-11-1992	US 5221413 A	22-06-1993
		JP 2792785 B	03-09-1998
		JP 6252046 A	09-09-1994
		US 5442205 A	15-08-1995
US 3905037 A	09-09-1975	FR 1546373 A	
		GB 1206159 A	23-09-1970